

Open Lounge Phone - minimal board v0.2 (RJ45 + PoE), schematic review

2-layer board, 156 x 88 mm. Pages 2-8: one page per block. Hardware docs: hardware/DESIGN.md.

Blocks

2. Power: USB-C (5 V sink + native USB), USB ESD, SGM2212 3.3 V LDO (8 parts)
3. MCU: ESP32-S3-WROOM-1U-N16R8, EN reset, RESET and BOOT buttons (7 parts)
4. Keys and hook: 13 MX hot-swap sockets, one GPIO each (internal pull-ups) (13 parts)
5. Audio: ES8311 codec + 3.5 mm TRRS handset jack (CTIA) (19 parts)
6. Display header, piezo ringer, status LED, board marking, mounting holes (7 parts)
7. Ethernet (v0.2): W5500 on the display SPI, its own 3.3 V LDO, RJ45 magnetics (36 parts)
8. PoE (v0.2): two bridges, TVS, isolated 802.3af DP9900LP-5V module, 3 mm isolation (9 parts)

Power tree

USB-C J1 VBUS (5 V, 5.1k Rd on CC1/CC2 = USB default power, no PD) -> B5819W D3 -> V5

RJ45 J4 PoE pairs -> MB10S BR1/BR2 -> SMAJ58A D4 -> DP9900LP-5V PS1 (isolated) -> POE_5V -> SS34 D5 -> V5

V5 -> SGM2212-3.3 U2 (800 mA LDO) -> 3V3: ESP32 module, ES8311, display module, mic bias, pull-ups, LED

V5 -> SGM2212-3.3 U5 -> ETH_3V3: W5500 digital, RJ45 LEDs; -> ferrite FB1 -> ETH_3V3A

-> piezo ringer BZ1 (through Q1, from V5 directly)

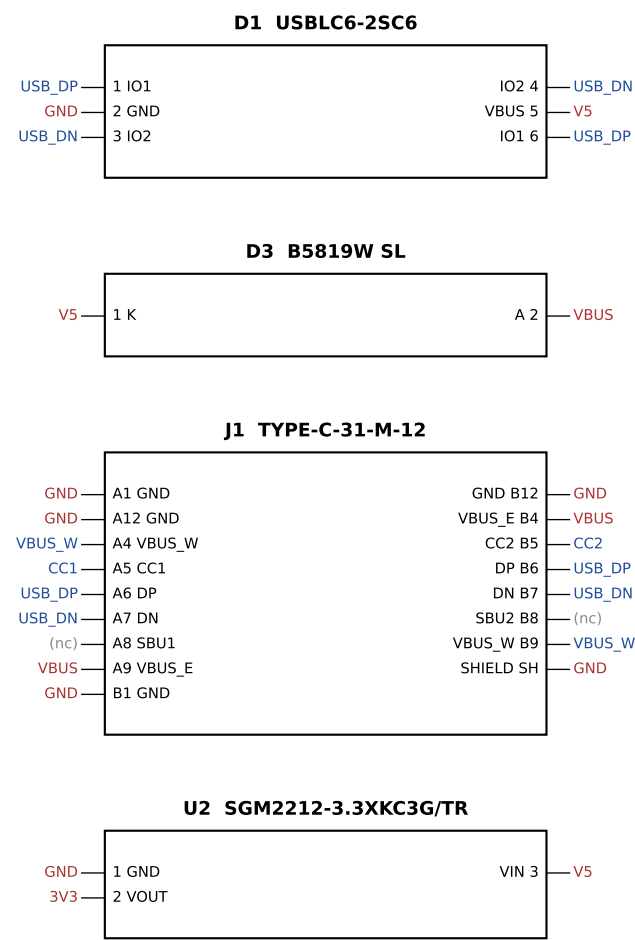
USB-C D+/D- -> USBLC6-2SC6 D1 -> ESP32 native USB (IO19/IO20): flashing + console

No fuse (compliant USB sources current-limit), no battery. USB and PoE diode-OR'd.

ESP32-S3 GPIO map (pin_table.yaml)

GPI00	ETH_CS	W5500 chip select (10k pull-up = SPI boot) + BOOT button through 1k (0.30 V at reset)
GPI01	STATUS_LED	front side, far left: LED at the band's front-left
GPI02	H00K	MX switch under the hook plunger: low = handset on the hook; RTC = deep-sleep wake
GPI03	KEY_1	JTAG-source strap, ignored unless EFUSE_STRAP_JTAG_SEL is burned (p15)
GPI04	JACK_DET	jack TN via 1k: low = no plug, high = plug in (internal pull-up)
GPI05	I2S_WS	
GPI06	I2S_BCLK	
GPI07	I2S_DIN	from ES8311 ASDOUT (record)
GPI08	BUZZER	NPN base via 1k (piezo next to the USB-C)
GPI09	KEY_3	
GPI010	KEY_4	
GPI011	KEY_5	
GPI012	KEY_MENU	
GPI013	EPD_CLK	
GPI014	EPD_DIN	
GPI015	I2S_DOUT	to ES8311 DSDIN (playback)
GPI016	I2S_MCLK	
GPI017	I2C_SCL	
GPI018	I2C_SDA	ES8311 only; 4.7k pull-up
GPI019	USB_DN	native USB D- (flashing + USB-Serial-JTAG console)
GPI020	USB_DP	native USB D+
GPI021	EPD_DC	
GPI035	(unconnected)	reserved: octal PSRAM
GPI036	(unconnected)	reserved: octal PSRAM
GPI037	(unconnected)	reserved: octal PSRAM
GPI038	EPD_RST	
GPI039	KEY_BACK	
GPI040	KEY_0	
GPI041	KEY_9	
GPI042	KEY_8	
GPI043	KEY_6	TXD0: the ROM boot log drives it for a moment after reset; a key held then only loses the l
GPI044	KEY_7	RXD0 (input at boot)
GPI045	ETH_MISO	W5500 MISO: Hi-Z while ETH_CS is high (W5500 p10), 10k pull-down; VDD_SPI strap must read l
GPI046	KEY_2	boot-mode strap (default low); a key can only pull it low
GPI047	EPD_CS	
GPI048	EPD_BUSY	

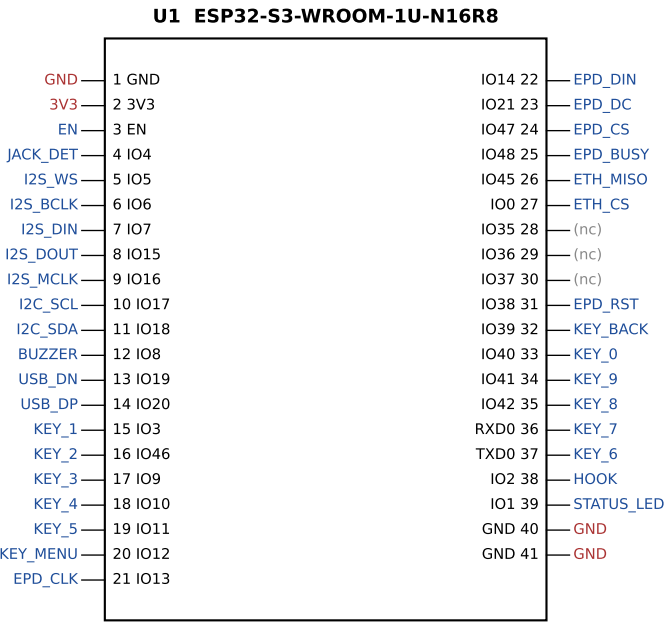
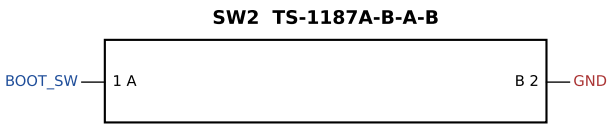
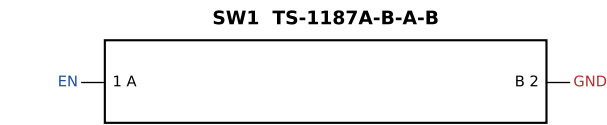
2. Power: USB-C (5 V sink + native USB), USB ESD, SGM2212 3.3 V LDO



Passives (ref, value, nets, note)

C1	4.7uF	16V X5R	V5 - GND	LD0 C_IN / V5 bulk (V5 total <= 10 uF: USB attach)
C2	2.2uF	16V X5R	3V3 - GND	LD0 C_OUT (SGM2212 p10)
R1	5.1k		CC1 - GND	Rd CC1
R2	5.1k		CC2 - GND	Rd CC2

3. MCU: ESP32-S3-WROOM-1U-N16R8, EN reset, RESET and BOOT buttons



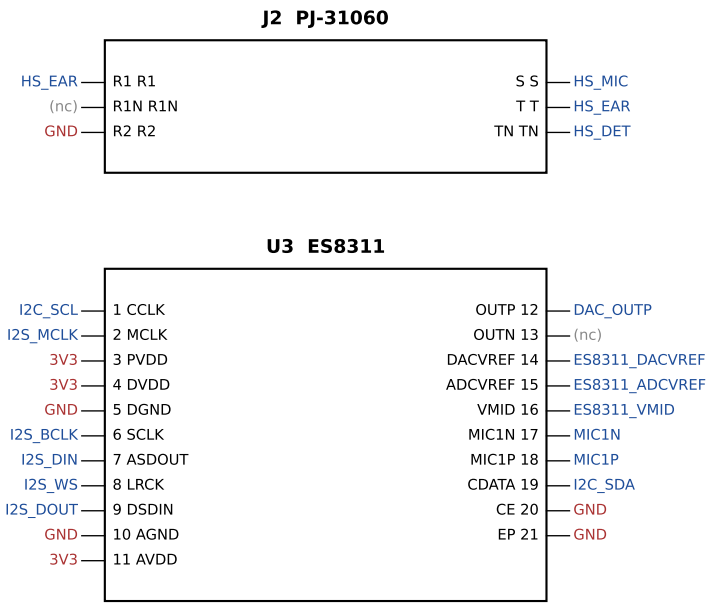
Passives (ref, value, nets, note)

C3	22uF 25V X5R	3V3 - GND	module 3V3 at pin 2 (WROOM-1 datasheet p41)
C4	100nF 50V X7R	3V3 - GND	module 3V3 at pin 2 (WROOM-1 datasheet p41)
C5	1uF 50V X5R	EN - GND	EN delay (p41)
R3	10k	EN - 3V3	EN pull-up (p41)

4. Keys and hook: 13 MX hot-swap sockets, one GPIO each (internal pull-ups)

Socket	pin 1 net	pin 2 net	note
SW3	KEY_1	GND	key 1
SW4	KEY_2	GND	key 2
SW5	KEY_3	GND	key 3
SW6	KEY_4	GND	key 4
SW7	KEY_5	GND	key 5
SW8	KEY_MENU	GND	key MENU
SW9	KEY_6	GND	key 6
SW10	KEY_7	GND	key 7
SW11	KEY_8	GND	key 8
SW12	KEY_9	GND	key 9
SW13	KEY_0	GND	key 0
SW14	KEY_BACK	GND	key BACK
SW15	H00K	GND	hook: MX switch pressed by the hook plunger

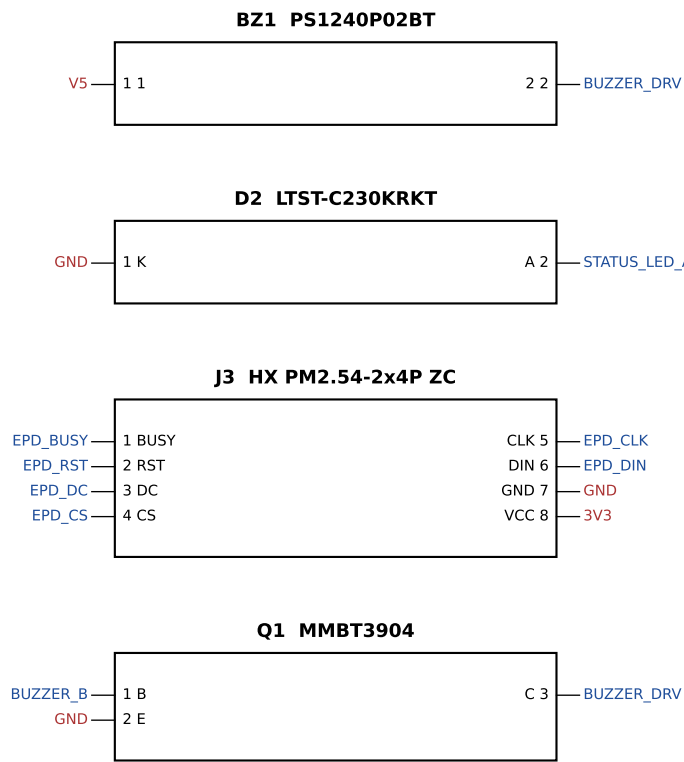
5. Audio: ES8311 codec + 3.5 mm TRRS handset jack (CTIA)



Passives (ref, value, nets, note)

C6	100nF	50V X7R	3V3 - GND	ES8311 PVDD, DVDD (p4)
C7	100nF	50V X7R	3V3 - GND	ES8311 PVDD, DVDD (p4)
C8	1uF	50V X5R	3V3 - GND	ES8311 AVDD (p4)
C9	1uF	50V X5R	ES8311_VMID - GND	VMID (p4)
C10	1uF	50V X5R	ES8311_ADCVREF - GND	ADCVREF (p4)
C11	1uF	50V X5R	ES8311_DACVREF - GND	DACVREF (p4)
C12	22uF	25V X5R	DAC_OUTP - EAR_AC	earpiece coupling: 22 uF into 32+22 ohm -> 134 Hz
C13	10uF	10V X5R	MIC_BIAS - GND	mic bias RC filter (16 Hz)
C14	1uF	50V X5R	HS_MIC - MIC1P	mic coupling (p4)
C15	1uF	50V X5R	MIC1N - GND	MIC1N reference (p4)
R4	4.7k		I2C_SDA - 3V3	I2C pull-up
R5	4.7k		I2C_SCL - 3V3	I2C pull-up
R6	22		EAR_AC - HS_EAR	earpiece series: plug-in short protection
R7	4.7k		HS_EAR - GND	tip DC reference: keeps the cap at 0 V, TN reads low
R8	1k		3V3 - MIC_BIAS	mic bias RC filter
R9	2.2k		MIC_BIAS - HS_MIC	electret bias
R10	1k		HS_DET - JACK_DET	GPIO series (contact reaches the plug)

6. Display header, piezo ringer, status LED, board marking, mounting holes

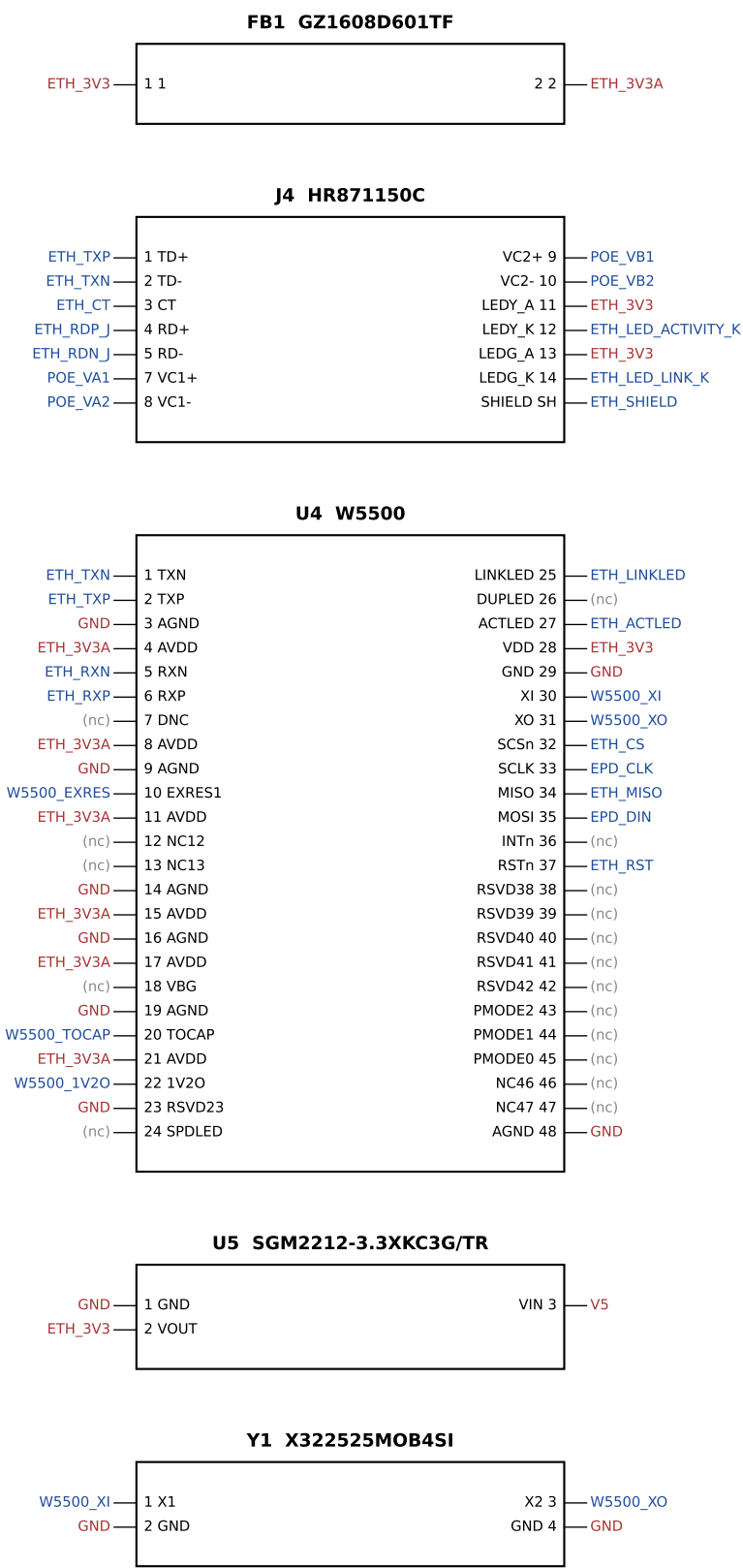


Passives (ref, value, nets, note)

R11	1k	V5 - BUZZER_DRV	piezo charge/discharge (TDK PS p2)
R12	1k	BUZZER - BUZZER_B	base resistor
R13	1k	STATUS_LED - STATUS_LED_A	status LED current (~1.5 mA)

No-pin items (layout only): G1 signature logo, G2 Open Lounge Phone, H1 M3 mounting hole, H2 M3 mounting hole, H3 M3 mounting hole, H4 M3 mounting hole, H5 M3 display standoff, H6 M3 display standoff

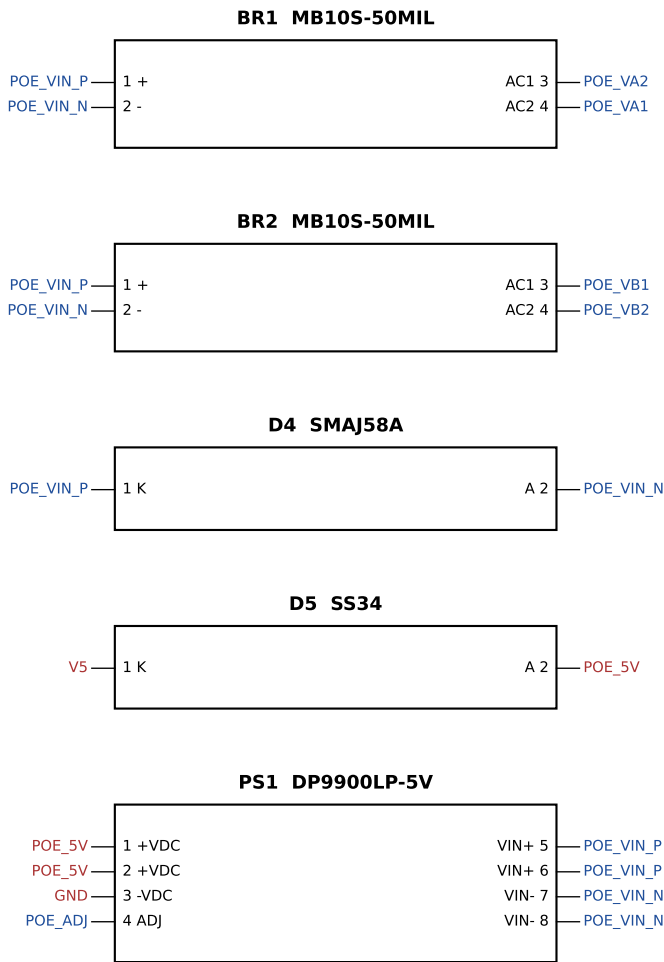
7. Ethernet (v0.2): W5500 on the display SPI, its own 3.3 V LDO, RJ45 magnetics



Passives (ref, value, nets, note)

C16	4.7uF 16V X5R	V5 - GND	Ethernet LDO C_IN (V5 total <= 10 uF: USB attach)
C17	2.2uF 16V X5R	ETH_3V3 - GND	Ethernet LDO C_OUT (SGM2212 p10)
C18	10uF 10V X5R	ETH_3V3 - GND	W5500 VDD pin 28
C19	100nF 50V X7R	ETH_3V3 - GND	W5500 VDD pin 28
C20	10uF 10V X5R	ETH_3V3A - GND	W5500 AVDD bulk
C21	100nF 50V X7R	ETH_3V3A - GND	W5500 AVDD (east pins 8/11, south 15/17, 21)
C22	100nF 50V X7R	ETH_3V3A - GND	W5500 AVDD (east pins 8/11, south 15/17, 21)
C23	100nF 50V X7R	ETH_3V3A - GND	W5500 AVDD (east pins 8/11, south 15/17, 21)
C24	4.7uF 16V X5R	W5500_TOCAP - GND	TOCAP (p8)
C25	10nF 50V X7R	W5500_1V20 - GND	1V20 (p8)
C26	18pF 50V C0G	W5500_XI - GND	crystal load
C27	18pF 50V C0G	W5500_XO - GND	crystal load
C28	4.7uF 16V X5R	ETH_RST - GND	RSTn power-on RC: ~47 ms, past the strap window
C29	6.8nF 50V X7R	ETH_RDP_J - ETH_RXP	RX+ AC coupling (joined centre tap)
C30	6.8nF 50V X7R	ETH_RDN_J - ETH_RXN	RX- AC coupling (joined centre tap)
C31	10nF 50V X7R	ETH_RXC - GND	RX termination centre
C32	100nF 50V X7R	ETH_CT - GND	centre-tap bypass
C33	1nF 2kV X7R	ETH_SHIELD - GND	RJ45 shield to GND (2 kV)
R14	1k	ETH_CS - BOOT_SW	BOOT button series (GPIO0 is also ETH_CS)
R15	12.4k	W5500_EXRES - GND	EXRES1 12.4 k 1 % (p11)
R16	1M	W5500_XI - W5500_XO	crystal bias (W5500 p11)
R17	10k	ETH_CS - ETH_3V3	ETH_CS pull-up: high at reset (SPI boot, MISO Hi-Z)
R18	10k	ETH_MISO - GND	ETH_MISO pull-down: GPIO45 strap low at reset
R19	10k	ETH_RST - ETH_3V3	RSTn power-on RC (no free GPIO)
R20	49.9	ETH_TXP - ETH_3V3A	TX+ termination (WIZnet ref)
R21	49.9	ETH_TXN - ETH_3V3A	TX- termination (WIZnet ref)
R22	49.9	ETH_RXP - ETH_RXC	RX termination
R23	49.9	ETH_RXN - ETH_RXC	RX termination
R24	10	ETH_3V3A - ETH_CT	centre-tap feed (WIZnet joined-CT ref)
R25	330	ETH_LED_LINK_K - ETH_LINKLED	RJ45 link LED
R26	330	ETH_LED_ACTIVITY_K - ETH_ACTLE	RJ45 activity LED

8. PoE (v0.2): two bridges, TVS, isolated 802.3af DP9900LP-5V module, 3 mm isolation



Passives (ref, value, nets, note)

C34	CA45-D-16V-100	P0E_5V - GND	PoE module output (≥ 100 uF low ESR, p3)
C35	10uF 25V X5R	P0E_5V - GND	PoE module output (p3)
R27	100k	P0E_ADJ - GND	ADJ to -VDC: 5.27 V (DP9900 p4)
R28	51	P0E_5V - GND	minimum-load bleeder (100 mA, p6): fit if the board idles below it